

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
7 August 2003 (07.08.2003)

PCT

(10) International Publication Number
WO 03/065778 A1

(51) International Patent Classification⁷: **H05K 1/18, 3/46**

(21) International Application Number: **PCT/FI03/00064**

(22) International Filing Date: 28 January 2003 (28.01.2003)

(25) Filing Language: Finnish

(26) Publication Language: English

(30) Priority Data:
20020190 31 January 2002 (31.01.2002) FI

(71) Applicant (for all designated States except US): **IMBERA ELECTRONICS OY** [FI/FI]; P.O. Box 74, FIN-02151 Espoo (FI).

(81) Designated States (*national*): AE, AG, AL, AM, AT (utility model), AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ (utility model), CZ, DE (utility model), DE, DK (utility model), DK, DM, DZ, EC, EE (utility model), EE, ES, FI (utility model), FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK (utility model), SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

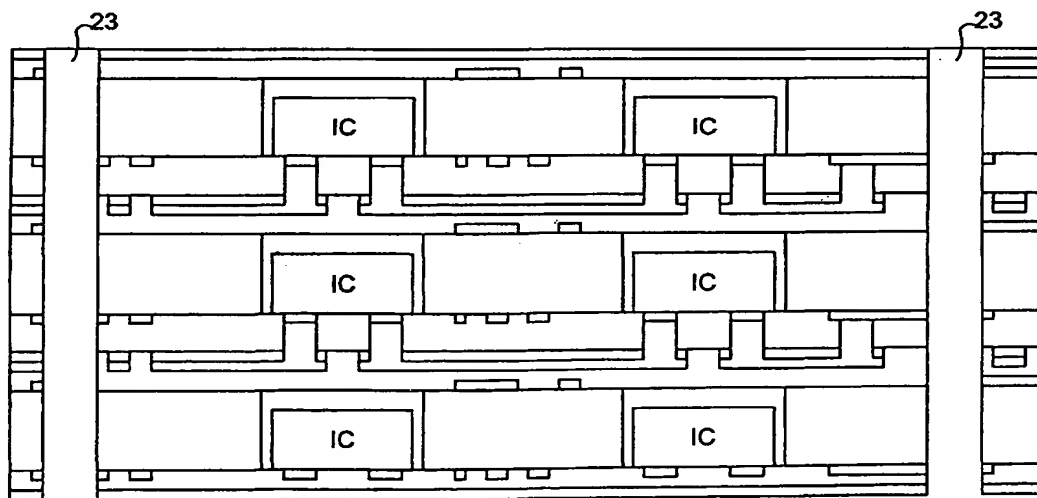
(72) Inventor; and
(75) Inventor/Applicant (for US only): **TUOMINEN, Risto** [FI/FI]; Väinöläkatu 17 B 18, FIN-00610 Helsinki (FI).

Published:
— with international search report

(74) Agent: **SEPPO LAINE OY**; Itämerenkatu 3 B, FIN-00180 Helsinki (FI).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: **METHOD FOR EMBEDDING A COMPONENT IN A BASE AND FORMING A CONTACT**



(57) Abstract: This publication discloses a method, in which the semiconductor components forming part of an electronic circuit, or at least some of them, are embedded in a base, such as a circuit board, during the manufacture of the base. Thus, the base structure is more or less manufactured around the semiconductor component. According to the invention, first of all at least one conductive pattern and through holes for the semiconductor components are made in the base. After this, the semiconductor components are placed in the holes in alignment with the conductive pattern. The semiconductor components are attached to the structure of the base and one or more conductive pattern layers are made in the base in such a way that at least one conductive pattern forms an electrical contact with the contact areas of the surface of the semiconductor component.

BEST AVAILABLE COPY



WO 03/065778 A1

METHOD FOR EMBEDDING A COMPONENT IN A BASE AND FORMING A CONTACT

5 The present invention relates to a method for embedding one or more components in a base and for forming contacts in them.

10 The bases that are processed using the methods to which the present invention relates are used as bases for electrical components, typically semiconductor components and particularly microcircuits, in electronic products. The task of the base is to provide a mechanical attachment base for the components and the necessary electrical connections to the other components on the base and outside the base. The base can be a circuit board, so that the method that is the object of the invention is closely related to circuit-board manufacturing technology. The base can also be some other base, for example, a base used for packaging a component or components, or the base of an entire functional module.

15 Circuit-board manufacturing technologies differ from microcircuit manufacture in, among other things, the fact that the substrate used in microcircuit manufacturing technologies is a semiconductor material, whereas the base material of a circuit board is an insulator. Microcircuit manufacturing technologies are also typically considerably more expensive than circuit-board manufacturing technologies.

20 Circuit-board manufacturing technologies differ from packaging techniques in that packaging techniques are intended to form a package around a semiconductor component, which will facilitate its handling. The surface of a package of a semiconductor component has contact parts, typically protrusions, which allow the packaged component to be easily installed on a circuit board. A semiconductor package also contains conductors, through which voltage can be connected to the actual semiconductor, connecting the protruding contact parts outside the package to the contact areas on the surface of the semiconductor component.

25 However, the packages of components manufactured using conventional technologies take up a considerable amount of space. The miniaturization of electronic devices has

led to an attempt to eliminate the packaging of semiconductor components. For this purpose, the so-called flip-chip technology for instance, has been developed, in which a semiconductor component without a package is assembled directly onto the surface of the circuit board. There are, however, many difficulties in flip-chip technology. For example, problems can arise with the reliability of connections, especially in applications in which mechanical stresses arise between the circuit board and the semiconductor component. Mechanical stresses must be evened by adding a suitable underfill between the chip and the circuit board. This procedure slows down the process and increases manufacturing costs. Stresses arise particularly in applications in which a flexible circuit board is used and the circuit board is flexed strongly.

Object of the invention is to create a method, by means of which unpacked microcircuits can be attached to a base and provided with contacts reliably but economically.

The invention is based on embedding the semiconductor components, or at least some of them, in a base, such as a circuit board, during the manufacture of the base, whereby part of the base structure is, as it where, manufactured around the semiconductor components. According to the invention, at least one conductive pattern is first manufactured in the base, as are through holes for the semiconductor components. After this, the semiconductor components are placed in the holes, in alignment with the conductive pattern. The semiconductor components are attached to the structure of the base and one or more layers of conductive patterns are manufactured in the base, in such a way that at least one conductive pattern forms an electrical contacts with the contact areas on the surface of the semiconductor component.

More specifically, the method according to the invention is characterized by what is stated in the characterizing portion of Claim 1.

Considerable advantages are gained with the aid of the invention. This is because, with the aid of the invention, a circuit board can be manufactured with the semiconductor components embedded inside it. The invention also makes it possible to manufacture a small and reliable component package around a component.

The invention also permits a large number of embodiments, which provide significant additional advantages.

For example, by means of the invention, the component's packaging stage, the circuit
5 board's manufacturing stage, and the assembly and contact-making stage of the
semiconductor components can be combined to form a single totality. The combination
of the various process stages brings important logistic benefits and permits the
manufacture of a smaller and more reliable electronic module. There is the further
advantage that such a manufacturing method can largely exploit circuit board
10 manufacturing and assembly technologies that are in general use.

The composite process according to a preferred embodiment of the invention is, in its
totality, simpler than, for example, manufacturing a circuit board and using flip-chip
technology to attach the components to the circuit board. By means of such preferred
15 embodiments, the following advantages over the conventional solution are obtained:

- Soldering is not required to form contacts with the components, instead an
electrical contact can be manufactured by growing conductors on top of the
contact areas of a semiconductor component. This means that there is no need to
20 use molten metal to connect the components, so that compounds are not formed
between metals. Compounds between metals are generally brittle, so that
reliability is improved compared to connections made by soldering. Particularly
in small connections, the brittleness of the metal compounds in the connections
causes great problems. According to a preferred embodiment, it is possible to
25 achieve clearly smaller structures in a solderless solution than in soldered
solutions. The solderless contact-making method also has the advantage that high
temperatures are not required to form contacts. A lower process temperature
permits greater choice when selecting other materials of the circuit board, the
component package, or the electronics module. In the method, the temperature of
30 the circuit board, the component, and the conductive layer directly connected to
the component can be kept in the range 20 - 85°C. Higher temperatures, for
example, of about 150°C, may be needed only when hardening (polymerizing)
any polymer films used. However, the temperature of the baseboard and the

components can be kept under 200°C during the entire process. In the method, it is also possible to use polymer films, which are hardened in other ways than due to the effect of a high temperature, for example, chemically, or by electromagnetic radiation, such as ultraviolet light. In such a preferred embodiment of the invention, the temperature of the baseboard and the components can be kept under 100°C during the entire process.

- Because the use of the method permits the manufacture of smaller structures, the components can be spaced more closely. The conductors between the components can then also be shorter while the electrical properties of the electronic circuit improve, for example, by reducing losses, interference, and delay times.

- The method also permits the manufacture of three-dimensional structures, as the bases and the components embedded in the bases can be assembled on top of each other.

- In the method, it is also possible to reduce the interfaces between different metals.

- The method permits a lead-free process.

The invention also permits other preferred embodiments. In connection with the invention, flexible circuit boards, for instance, can be used. Further, the process permits circuit boards to be assembled on top of each other.

With the aid of the invention, it is also possible to manufacture extremely thin structures, in which the semiconductor components are, despite its thinness, entirely protected within a base, such as a circuit board.

Because the semiconductor components can be placed entirely inside the circuit board, the joints between the circuit board and the semiconductor components are mechanically durable and reliable.

In the following, the invention is examined with the aid of examples and with reference to the accompanying drawings.

5 Figure 1 shows a series of cross-sections of one process according to the invention.

Figure 2 shows a series of cross-sections of a second process according to the invention.

10 Figure 3 shows a series of cross-sections of a third process according to the invention.

The series of illustrations shown in Figure 1 show one possible process according to the invention. In the following, the process of Figure 1 is examined in stages:

Stage A (Figure 1A):

15

In stage A, a suitable baseboard 1 is selected for the circuit-board manufacturing process. The baseboard 1 can be, for example, a glass-fibre reinforced epoxy board, such as an FR4-type board. In the example process, the baseboard 1 can thus be an organic board, as the example process does not require high temperatures. A flexible and cheap
20 organic board can thus be selected for the baseboard 1. Typically a board that is already coated with a conductive material 2, usually copper, is selected for the baseboard 1. Of course, an inorganic board can also be used.

Stage B (Figure 1B):

25

In stage B, through holes 3 are made in the baseboard for electrical contacts. The holes 3 can be made, for example, with some known method used in circuit-board manufacture, such as mechanical drilling.

30 **Stage C (Figure 1C):**

In stage C, metal 4 is grown into the through holes made in stage B. In the example process, the metal 4 is also grown on top of the circuit board, thus also increasing the

thickness of the conductive layer 2.

5 The conductive material 4 to be grown is copper, or some other material with sufficient electrical conductivity. Copper metallizing can take place by coating the holes with a thin layer of chemical copper and then continuing the coating using an electrochemical copper-growing method. Chemical copper is used in the example, as it will also surface on top of a polymer and act as an electrical conductor in electrochemical coating. The metal can thus be grown using a wet-chemical method, so that the growth is cheap. Alternatively, the conductive layer 4 can be made, for example, by filling the through
10 holes with an electrically conductive paste.

Stage D (Figure 1D):

15 In stage D, the conductive layer on the surface of the circuit board is patterned. This can be done by utilizing generally known circuit-board manufacturing methods. The patterning of the conductive layer is aligned, for example, on the holes made in stage B.

The manufacture of the conductor pattern can take place, for example, by laminating, on the surface of the metal 4, a photolithographic polymer film, on which the desired
20 conductive pattern is formed by directing light through a patterned mask. After exposure, the polymer film is developed, when the desired areas are removed from it and the copper 4 under the polymer is revealed. Next, the copper revealed under the film is etched away, leaving the desired conductive pattern. The polymer acts as a so-called etching mask and openings 5, at the foot of which the baseboard of the circuit board is
25 revealed, are formed in the metal layer 4. After this, the polymer film is also removed from on top of the copper 4.

Stage E (Figure 1E):

30 In stage E, holes 6 are made in the baseboard for the microcircuits. The holes extend through the entire baseboard, from the first surface 1a to the second surface 1b. The holes may be made, for example, mechanically milling by means of a milling machine. The holes 6 can also be made, for example, by stamping. The holes 6 are aligned relative

to the conductive patterns 4 of the circuit board. The holes 3 made during stage B can also be used to aid alignment, but then too the alignment is relative to the conductive patterns 4, as the conductive patterns 4 have a specific position in relation to the holes 3.

5 **Stage F (Figure 1F):**

In stage F, tape 7 or similar is laminated over the holes 6. The tape 7 is laminated by stretching it straight over the hole 6 along the second surface 1b of the baseboard. The tape is intended to hold the components to be assembled in the next stage in place, until
10 the components have been secured to the baseboard using the final attachment method.

Stage G (Figure 1G):

In stage G, the microcircuits 8 are assembled in the holes 6, from the side of the first
15 surface 1a of the baseboard. Assembly can take place using a precision assembly machine, the microcircuits 8 being aligned relative to the conductive patterns of the circuit board. As in stage E, the holes made in stage B can be used to aid alignment.

The microcircuits 8 are assembled in such a way that they adhere to the adhesive surface
20 of the tape 7 in the 'bottoms' of the holes 6.

Stage H (Figure 1H):

In stage H, the microcircuits 8 are attached to the baseboard of the circuit board by using
25 a filler substance 9 to fill the holes made for the microcircuits. In the example process, this stage is carried out by spreading casting epoxy into the holes and on top of the microcircuits 7, from the side of the first surface (1a) of the circuit board. The epoxy is smoothed with a spatula and is hardened by curing in an autoclave.

30 **Stage I (Figure 1I):**

In stage I, the tape laminated in stage F is removed.

Stage J (Figure 1J):

In stage J, a polymer film 10 is formed on the surface of the circuit board, followed by a thin metal coating 11 on top of the polymer film. The film is preferably formed on both
5 surfaces of the circuit board, but at least on the second surface (1b) of the circuit board.

In the example process, stage J is carried out by laminating a thin polymer film (e.g., c. 40 μm) on the surface of the circuit board, on top of which is a layer of copper (e.g., c. 5 μm). Lamination takes place with the aid of pressure and heat. In the example process,
10 the film is thus an RCC (Resin Coated Copper) foil.

The polymer film can also be made by, for example, spreading polymer in a liquid form on the circuit board. Thus lamination is not essential in stage J. What is essential is that an insulating layer, typically a polymer film, is made on the circuit board, which
15 contains the embedded components, particularly embedded microcircuits. The polymer film itself can be, according to the embodiment, a filled or unfilled polymer film. The polymer film can also be coated with metal, but this is not essential, as the conductive surface can also be made later, on top of a polymer layer that is already attached to the circuit board.

20

Stage J makes it possible to use conventional manufacturing methods and work stages used in circuit board manufacture in the example process and nevertheless to be able to bury microcircuits and other components inside the circuit board.

25 Stage K (Figure 1K)

In stage K, holes 12 are made in the polymer film 10 (and at the same time in the conductive foil 11), through which it is possible to create contacts with the conductive patterns and feed-throughs (conductive material 4) of the circuit board and with the
30 microcircuits 8.

The holes 12 can be made, for example, using a laser, or some other suitable method. The conductive patterns made in stage D, or the through holes made in stage B can be

used for alignment.

Stage L (Figure 1L):

Stage L corresponds to stage C. In stage L, a conductive layer 13 is made in the holes 12 and on the surfaces of the circuit board.

In the example process, the feed-throughs (holes 12) are first of all cleaned using a three-stage desmear treatment. After this, the feed-throughs are metallized by first forming a catalysing SnPd surface on the polymer and after that depositing a thin layer (about 2 Fm) of chemical copper onto the surface. The thickness of the copper 13 is increased by electrochemical deposition.

Alternatively, the feed-throughs can be filled with an electrically conductive paste or made using some other suitable micro-via metallizing method.

Stage M (Figure 1M):

In stage M, a conductive pattern is formed in the same way as in stage D.

Stages N and O (Figures 1N and 1O):

In stages N and O, a photolithographic polymer 14 is spread on the surfaces of the circuit board and the desired pattern is formed in the polymer 14 (in a manner similar to that in stages D and M). The exposed polymer film is developed, but the polymer film pattern remaining on the circuit board is not removed.

Stage P (Figure 1P):

In stage P, the connection areas of the polymer film pattern formed in the previous stage are coated 15. The coating 15 can be made with, for example, a Ni/Au coating, or an OSP (organic surface protection).

The example of Figure 1 depicts one process, which can be used to exploit our invention. Our invention is thus in no way restricted to the process described above, but instead the invention covers a large group of different processes and their end products, to the full extent of the Claims and allowing for equivalency interpretations. In particular, the invention is in no way restricted to the layout shown in the example, instead it will be obvious to one versed in the art that the processes according to our invention can be used to manufacture many kinds of circuit boards, which differ greatly from the examples disclosed here. Thus, the microcircuits and connections of the figures are only shown to illustrate the manufacturing process. A great many changes can thus be made to the process of the example disclosed above, without nevertheless deviating from the idea according to the invention. The changes can relate to the manufacturing techniques depicted in the various stages, or, for example, to the mutual sequence of the stages. For example, stage B can equally well be carried out after stage D, i.e. the procedure can be to align the drill on the pattern, instead of aligning the pattern on the drilled holes.

Stages that are felt to be required can also be added to the process of the example disclosed above. For example, a foil that protects the surface of the circuit board during the casting taking place in stage H can be laminated onto the first side (1a) of the circuit board. Such a protective foil is manufactured so that it covers all the other areas except for the holes 6. The protective foil keeps the surface of the circuit board clean when the casting epoxy is spread with the spatula. The protective foil can be made in a suitable stage before stage H and is removed from the surface of the circuit board immediately after the casting.

With the aid of the method, it is also possible to manufacture component packets to be attached to the circuit board. Such packets can also include several semiconductor components, which are connected electrically to each other.

The method can also be used to manufacture entire electrical modules. The process shown in Figure 1 can also be applied in such a way that the conductive structure is made only on the second side (1b) of the circuit board, to which the contact surfaces of the microcircuit are oriented.

The method makes it possible to manufacture, for example, circuit boards or electrical modules, in which the thickness of the baseboard used is in the range 50 - 200 microns and the thickness of the microcircuit and microcircuits is in the range 50 - 150 microns. The pitch of the conductors can vary, for example, in the range 50 - 250 microns while the diameter of the micro-feed-throughs can be, for example, 15 - 50 microns. Thus, the total thickness of a single board in a one-layer construction will be about 100 - 300 microns.

The invention can also be applied in such a way that circuit boards are assembled on top of each other, thus forming a multi-layer circuit structure, in which there are several circuit boards manufactured according to Figure 1 set on top of each other and connected electrically to each other. The circuit boards set on top of each other can also be circuit boards in which the conductive structure is formed only on the second side 1b of the circuit board, but which nevertheless include feed-throughs, through which an electrical contact can also be formed to the microcircuits from the first side of the circuit board. Figure 2 shows one such process.

Figure 2 shows the connection of circuit boards to each other. In the following, the process is described in stages.

Stage 2A (Figure 2A):

Stage 2A depicts the circuit boards being set on top of each other. The lowest circuit board can be obtained, for example, after stage I of a modified process of Figure 1. In this case, the process of Figure 1 is then modified by omitting stage 1C.

The middle and upper circuit boards in turn can be obtained after stage M of a modified process of Figure 1, for instance. In this case, the process of Figure 1 is modified by omitting stage 1C and performing stages J, K, and L on only the second side (1b) of the circuit board.

In addition to the circuit boards, Figure 2A also shows pre-preg epoxy layers 21 placed

between the circuit boards.

Stage 2B (Figure 2B):

5 In stage 2B, the circuit boards are laminated together with the aid of pre-preg epoxy layers 21. In addition, a metal-coated polymer film 22 is made on both sides of the circuit board. The process corresponds to stage J of the process of Figure 1.

Stage 2C (Figure 2C):

10 In stage 2C, holes 23, for the formation of contacts, are drilled in the circuit board.

After Stage 2C, the process can be continued for example as follows:

15 **Stage 2D:**

In stage 2D, conductive material is grown on top of the circuit board and in the through holes 23, in the same way as in stage 1C.

20 **Stage 2E:**

In stage 2E, the conductive layer on the surface of the circuit board is patterned in the same way as in stage 1D.

25 **Stage 2F:**

In stage 2F, a photolithographic polymer is spread on the surfaces of the circuit board and the desired pattern is formed in the polymer in the same way as in stages 1N and 1O. The exposed polymer film is developed, but the polymer film pattern remaining on the
30 circuit board is not removed.

Stage 2G:

In stage 2G, the connection areas of the polymer film pattern formed in the previous stage are metallized in the same way as in stage 1P.

5 On the basis of the example of Figure 2, it is obvious that the method can also be used to manufacture many kinds of three-dimensional circuit structures: For example, the method can be used in such a way that several memory circuits are placed on top of each other, thus forming a packet containing several memory circuits, in which the memory
10 circuits are connected to each other to form an operational totality. Such a packet can be termed a three-dimensional multichip module. The chips in such modules can be selected freely and the contacts between the chips can be easily made according to the selected circuits.

The invention also permits electromagnetic protection to be made around the component
15 embedded in the base. This is because the method of Figure 1 can be modified in such a way that the holes 6 depicted in stage 1E can be made in connection with the making of the holes 3 carried out in stage 1B. In that case, the conductive layer 4 to be made in stage 1C will also cover the side walls of the holes 6 made for the components. Figure 3A shows a cross-section of the base structure as it is after stage 1F in the process
20 modified in the aforesaid manner.

After the intermediate stage shown in Figure 3A, the process can be continued by assembling the microcircuits in a similar way to stage 1G, the microcircuits being attached similarly to stage 1H, the tape removed similarly to stage 1I, and polymer and
25 metal foils being made on both surfaces of the circuit board in a similar way to stage 1J. Figure 3B shows an example cross-section of the base structure after these process stages.

After the intermediate stage shown in Figure 3B, the process can be continued by
30 making holes, similar to those of stage 1K, in the polymer film, for making contacts. After this, a conductive layer is made in the holes and on the surfaces of the board similarly to stage 1L. Figure 3C shows an example cross-section of the base structure after these process stages. For reasons of clarity, the conductive layer made similarly to

stage 1L in the holes and on the board surfaces is highlighted in black.

After the intermediate stage shown in Figure 3C, the process can be continued by patterning a conductive layer on the surfaces of the board as in stage 1M and by coating the surfaces of the board as in stage 1N. After these stages, the microcircuits are surrounded by a nearly unbroken metal foil, which forms an effective protection against interference caused by electromagnetic interaction. This construction is shown in Figure 3D. After the intermediate stage shown in Figure 3D, stages corresponding to stages 1O and 1P are carried out, in which a protective foil and connections are made on the surface of the circuit board.

In Figure 3D, the cross-sections of the metal layers protecting the microcircuits are highlighted in black. In addition, the background of the microcircuits is highlighted with cross-hatching. The cross-hatching is intended to be a reminder that all the sides of a hole made for a microcircuit are covered by a metal foil. Thus the microcircuit is surrounded laterally with an unbroken metal foil. In addition to this, a metal plate can be designed above the microcircuit, which is made in connection with the making of the circuit board's conductive pattern. Similarly, a metal foil that is as complete as possible is made below the microcircuit. The making of contacts below the microcircuit means that small gaps must be made in the metal foil, as shown in Figure 3D, for instance. These gaps can, however, be made so narrow laterally, or, correspondingly, so thin vertically, that they do not weaken the protective effect obtained against electromagnetic interference.

When examining the example of Figure 3D, it must also be taken into account that the final structure also contains parts extending at right angles to the plane shown in the figure. Such a structure extending at right angles is shown by the conductor connected to the contact bump on the left-hand side of the left-hand microcircuit of Figure 3D, which runs towards the viewer from between the metal foil surrounding the microcircuit laterally and the conductive layers below the microcircuit.

The solution shown by Figure 3D thus provides the microcircuit with excellent protection against electromagnetic interference. As the protection is made immediately

around the microcircuit, the construction also protects against mutual interference arising between the components contained in the circuit board. Most of the electromagnetic protective structure can also be earthed, as the metal foil surrounding the microcircuits laterally can be connected electrically to the metal plate above the circuit. The connections of the circuit board, can, in turn, be designed in such a way that the metal plate is earthed through the conductive structure of the circuit board.

Claims:

1. A method for embedding a component in a base and for forming electrical contacts with the component, the method comprising

5

- taking a baseboard as the base,
- making conductive patterns on the baseboard,
- making a hole in the baseboard in such a way that the position of the hole is selected in relation to the conductive patterns made on the baseboard,
- 10 - placing a component in the hole, in such a way that the component is aligned in relation to the conductive patterns made on the baseboard,
- securing the component in place in the hole made in the baseboard,
- making an insulating layer made on at least one surface of the base, in such a way that the insulating layer covers the component,
- 15 - making contact openings for the component in the insulating layer, and
- making conductors to the contact openings and on top of the insulating layer, in order to form electrical contacts with the component.

20

2. A method according to Claim 1, in which the hole, which is made in the baseboard of the circuit board for a component, is a through hole.

25

3. A method according to Claim 2, in which insulating material is grown on the side walls of the hole made for a component, in order to create interference protection around the component.

30

4. A method according to any of Claims 1 - 3, in which the component to be placed in the hole is a microcircuit, on the first surface of which there are contact areas or contact protrusions for creating electrical contacts.

5. A method according to Claim 4, in which, after making the hole

- tape or a tape-like film is laminated on the first side of the baseboard,
- the microcircuit is placed in the hole made in the baseboard from the second-

surface side of the baseboard, so that the first surface of the microcircuit lies against the tape or tape-like film and is essentially on the same level as the first surface of the baseboard, and

- the microcircuit is secured in place in the hole made in the baseboard by filling the hole with a filler material.

6. A method according to Claim 5, in which, after the securing of the microcircuit

- the tape or tape-like film laminated on the first surface of the baseboard is removed,

- an RCC foil is laminated onto the first surface of the baseboard, and

- conductive patterns and contact openings for the components are made in the RCC foil.

7. A method according to Claim 5, in which holes are made for feed-throughs and, after the securing of the microcircuit

- the tape or tape-like film laminated on the first surface of the baseboard is removed,

- RCC foils are laminated onto the first and second surfaces of the baseboard,

- conductive patterns and contact openings for the components and feed-throughs are made in the RCC foil laminated onto the first surface of the baseboard, and

- conductive patterns and contact openings for the feed-throughs are made in the RCC foil laminated onto the second surface of the baseboard.

8. A method according to Claim 5, in which, after the securing of the microcircuit

- the tape or tape-like film laminated on the first surface of the baseboard is removed,

- a pre-preg epoxy foil is made on the first surface of the baseboard,

- contact openings for the component are made in the epoxy foil, and

- conductive patterns are made on top of the epoxy foil.

9. A method according to Claim 5, in which holes for feed-throughs are made in the base, and, after the securing of the microcircuit

- 5 - the tape or tape-like film laminated on the first surface of the baseboard is removed;
- pre-preg epoxy foils are laminated onto the first and second sides of the baseboard;
- contact openings for the component and feed-throughs are made in the epoxy foil of the first surface of the baseboard, and
- 10 - contact openings for the feed-throughs are made in the epoxy foil of the second surface of the baseboard.

10. A method according to any of Claims 4 - 9, in which an electrical contact is formed with the microcircuit from the direction of the first surface of the baseboard, after the
15 microcircuit has been placed in the hole made in the baseboard.

11. A method according to any of Claims 4 - 10, in which an electrical contact is formed with the microcircuit by growing conductive material in the contact areas of the microcircuit, or on top of its contact protrusions.

20 12. A method according to any of Claims 4 - 11, in which the electrical contact with the microcircuit is formed without solder using a circuit-board manufacturing technology.

13. A method according to any of Claims 1 - 12, in which more than one component is
25 embedded in the base in a corresponding manner.

14. A method according to Claim 13, in which a separate hole is made in the baseboard for each component to be embedded in the base and each component to be embedded in the base is located in its own hole.

30 15. A method according to any of Claims 1 - 14, in which at least two microcircuits are embedded in the base, and in which a conductive layer is grown, which is connected directly to the contact areas or contact protrusions of at least two microcircuits, in order

to connect the microcircuits electrically to each other to form an operational totality.

16. A method according to any of Claims 1 - 15, in which a multi-layer structure is manufactured, in which there are at least four conductive layers on top of each other.

5

17. A method according to any of Claims 1 - 16, in which a first base and at least one second base are manufactured and the bases are assembled and secured on top of each other in such a way that the bases are aligned in relation to each other.

10

18. A method according to any of Claims 1 - 16, in which

- a first and a second base and an intermediate layer are manufactured,
- the second base is placed above the first base and the second base is aligned in relation to the first base,
- the intermediate layer is placed between the first and the second bases, and
- the first and second bases are laminated to each other with the aid of the intermediate layer.

15

19. A method according to Claim 18, in which

20

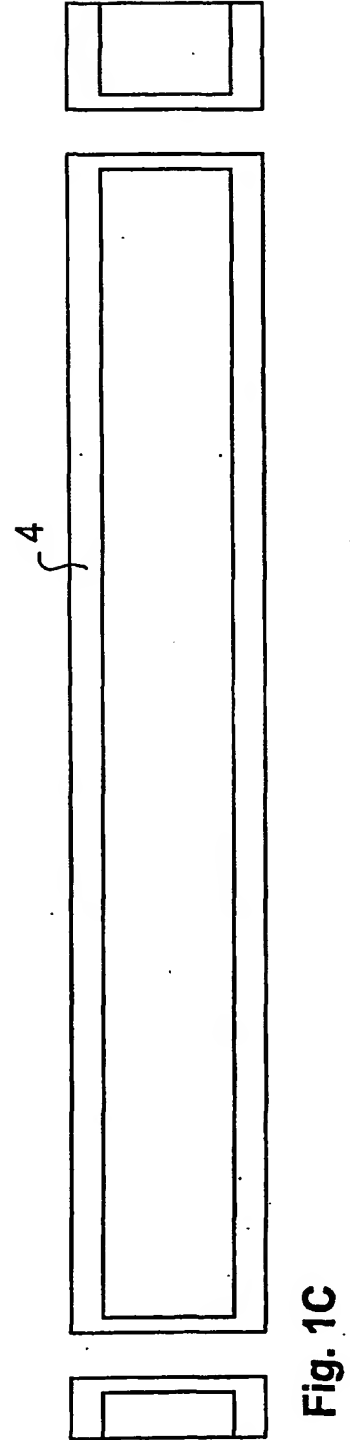
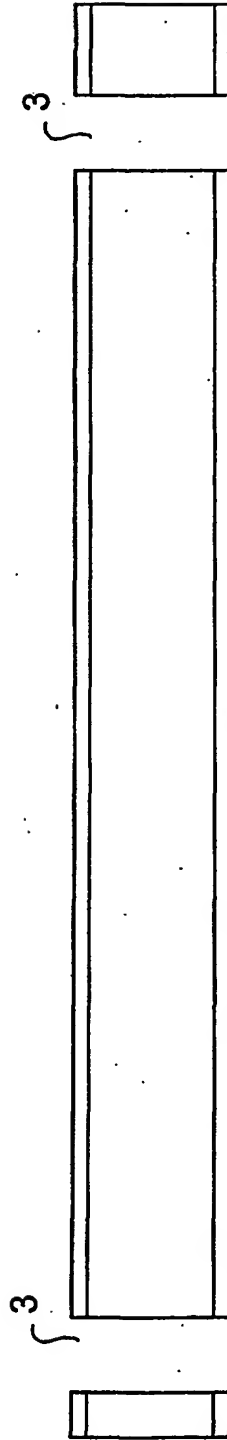
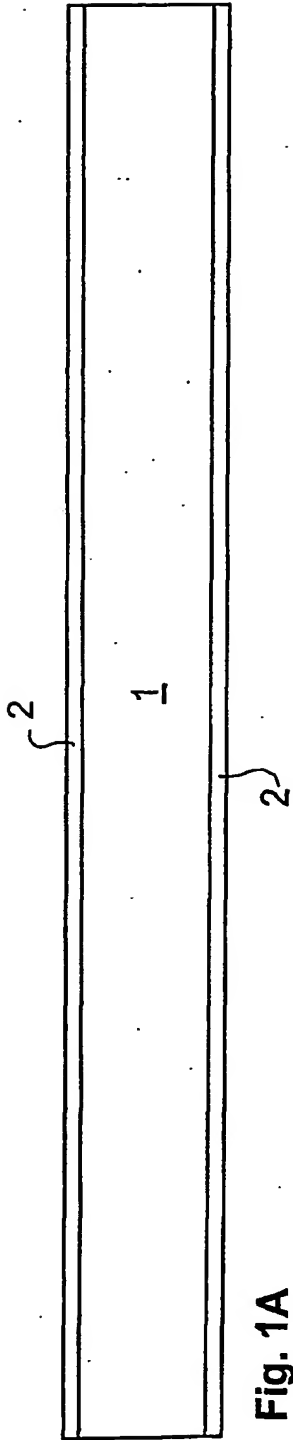
- at least one third base and an intermediate layer for each third base are manufactured,
- each third base is placed in turn above the first and second bases and each third base is aligned in relation to one of the lower bases,
- an intermediate layer is placed beneath each third base, and
- the first, second, and each third base are laminated to each other with the aid of the intermediate layers.

25

20. A method according to any of Claims 17 - 19, in which holes for feed-throughs are drilled through the bases secured on top of each other and conductors are made in the drilled holes for connecting the electronic circuits of each base to each other to form an operational totality.

30

21. A method according to any of Claims 1 - 20, in which the temperature of the baseboard, component, and conductive layer connected directly to the component, is, during the process, less than 200°C and preferably in the range 20 - 85°C.
- 5 22. An electronic module, which is manufactured using a method according to any of Claims 1 - 21.



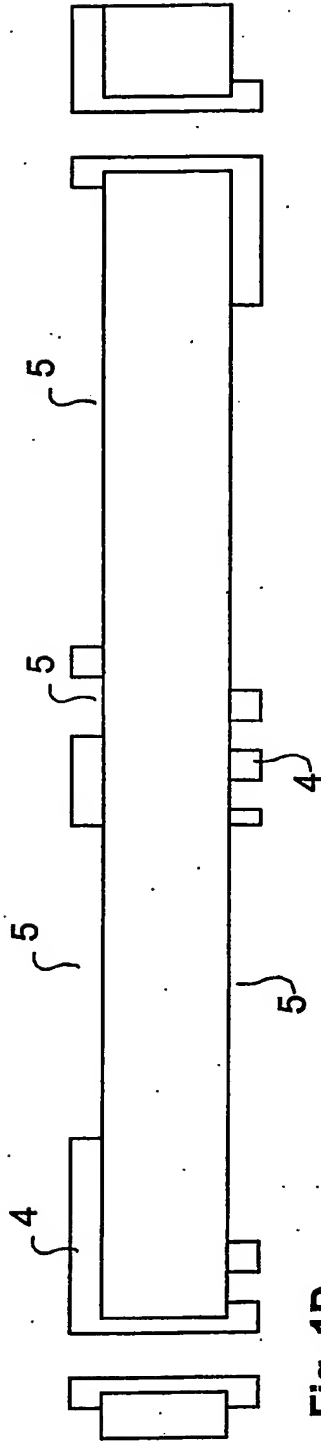


Fig. 1D

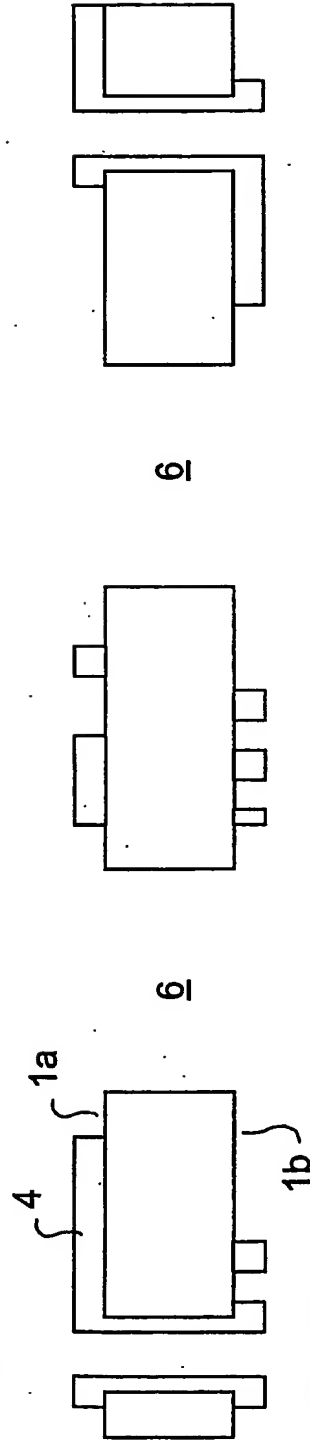


Fig. 1E

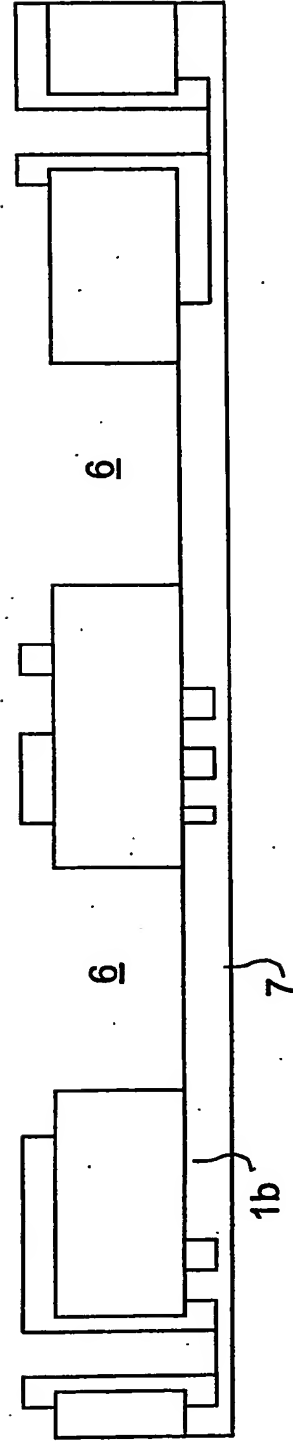


Fig. 1F

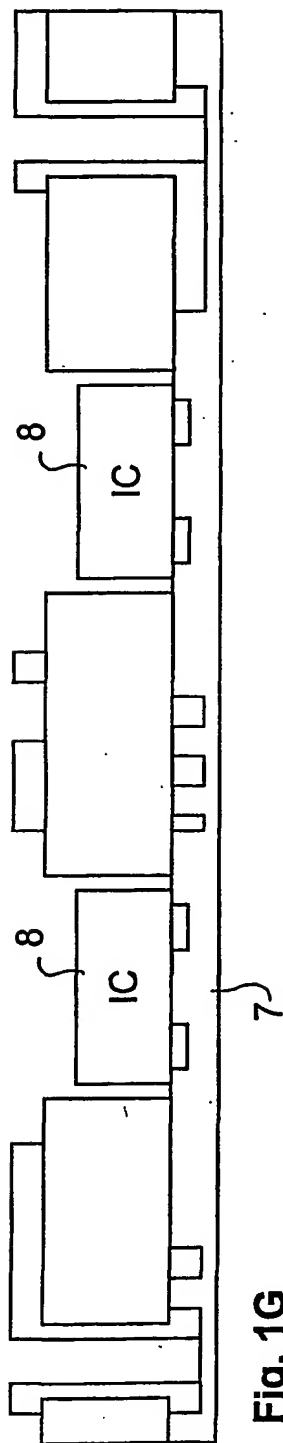


Fig. 1G

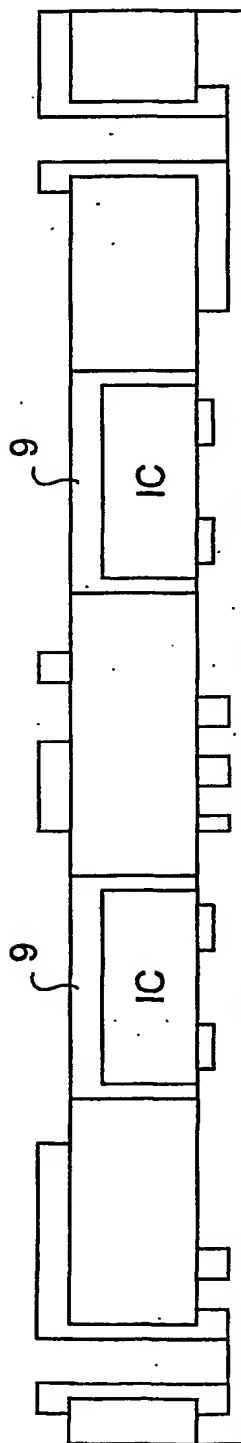


Fig. 1H

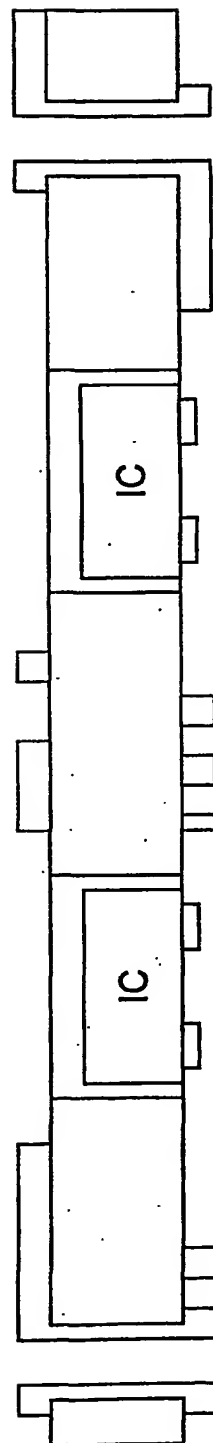


Fig. 1I

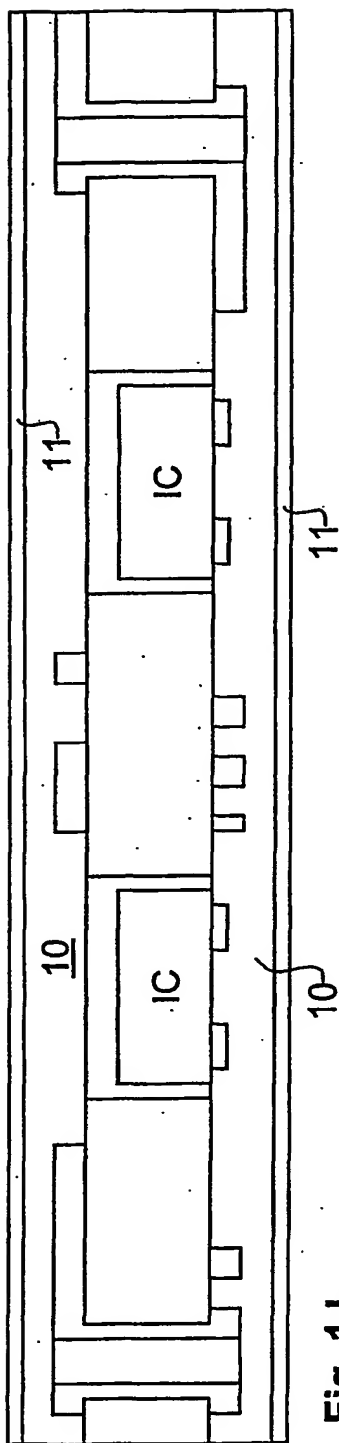


Fig. 1J

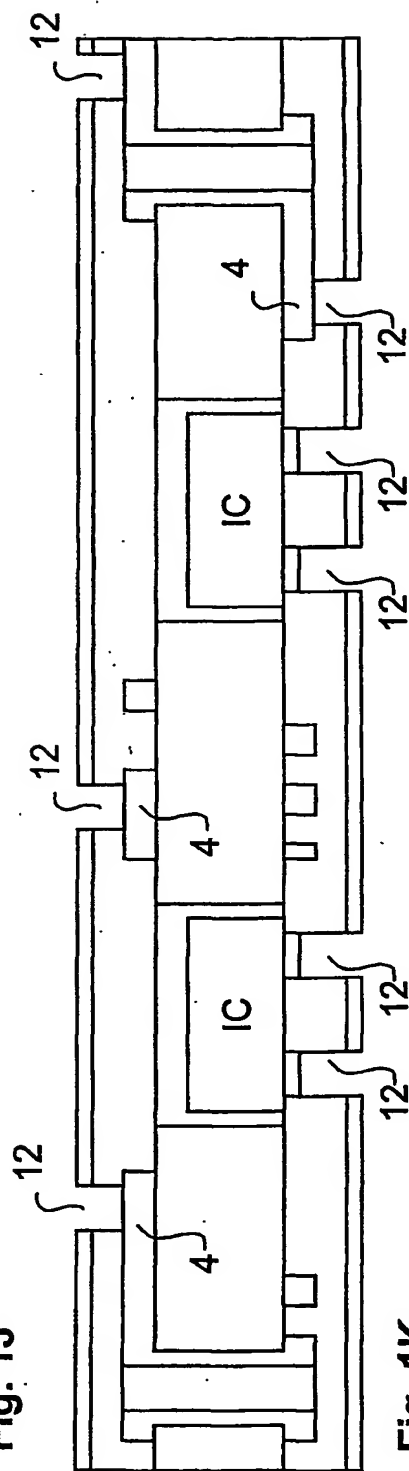


Fig. 1K

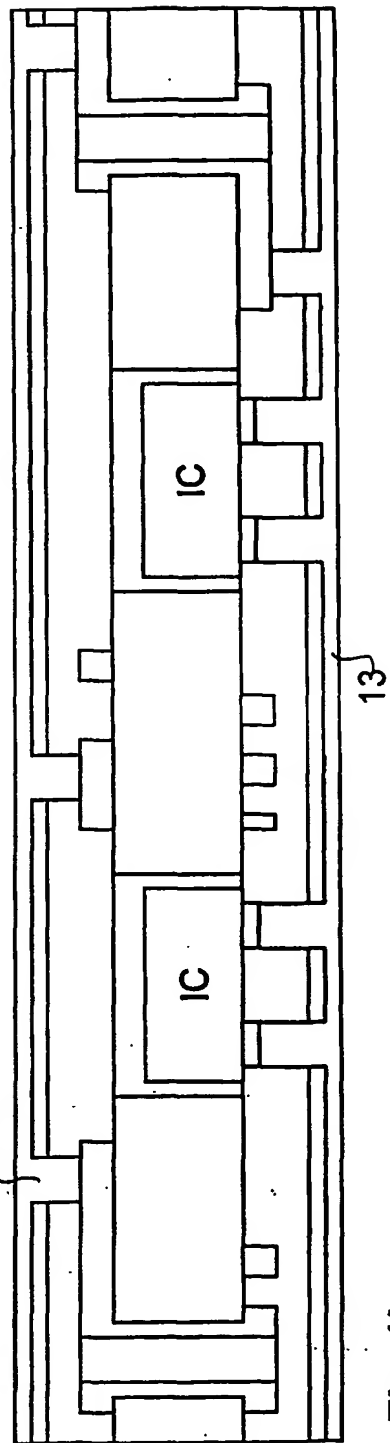
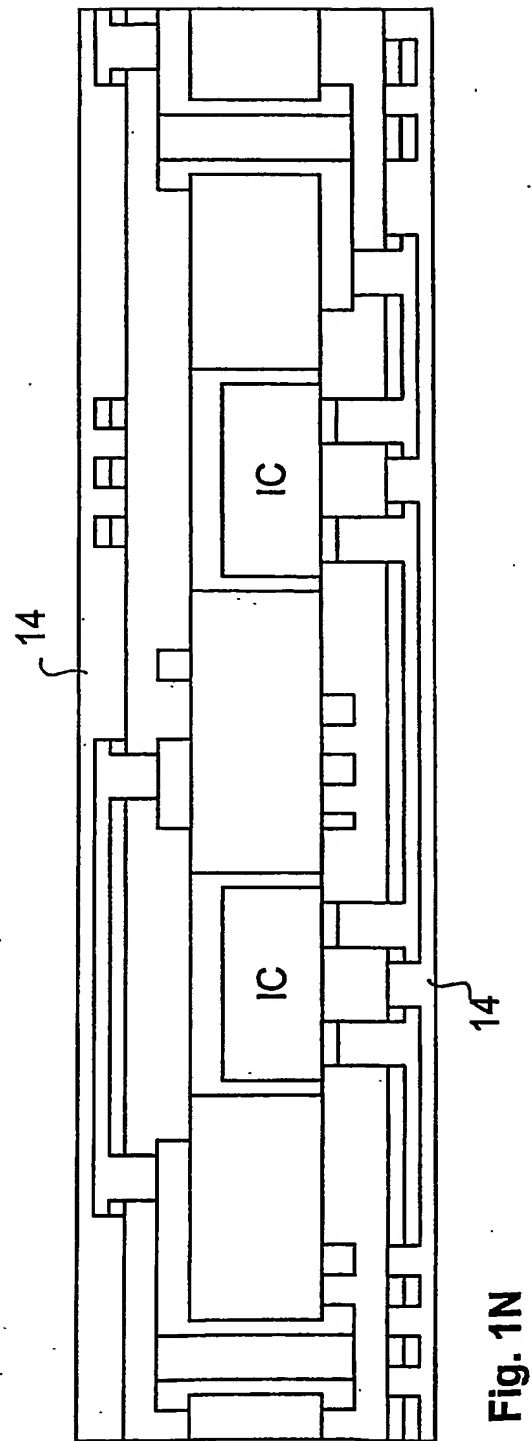
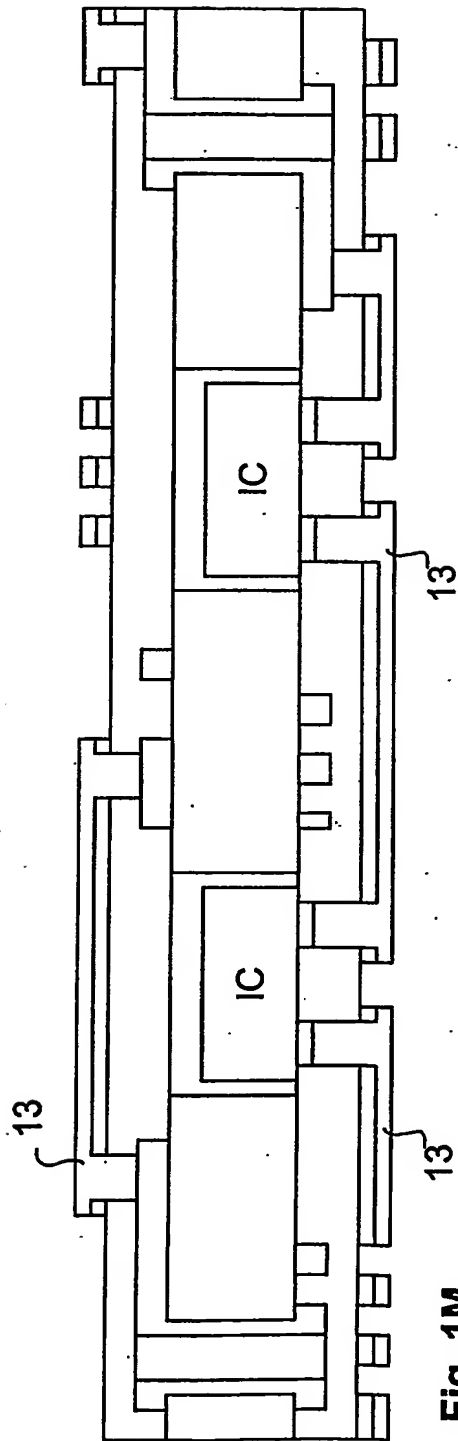


Fig. 1L



6/11

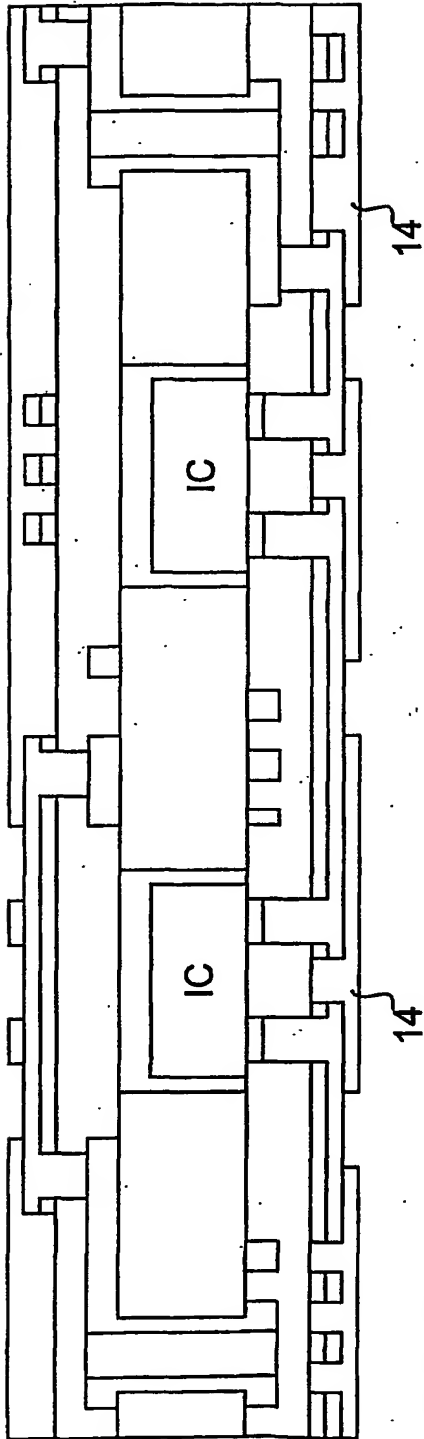


Fig. 10

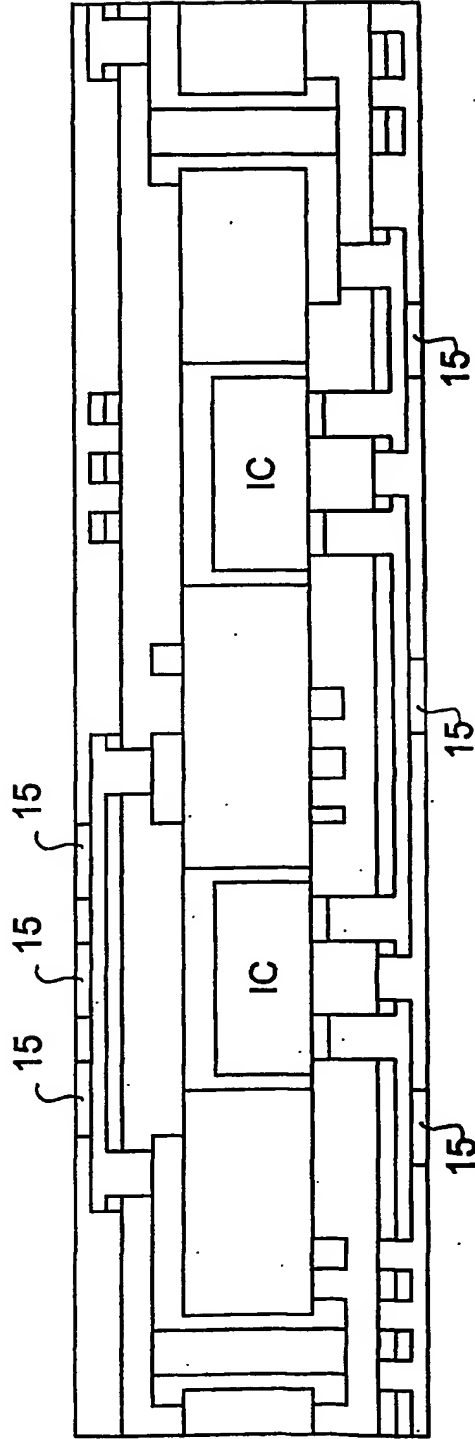


Fig. 1P

7/11

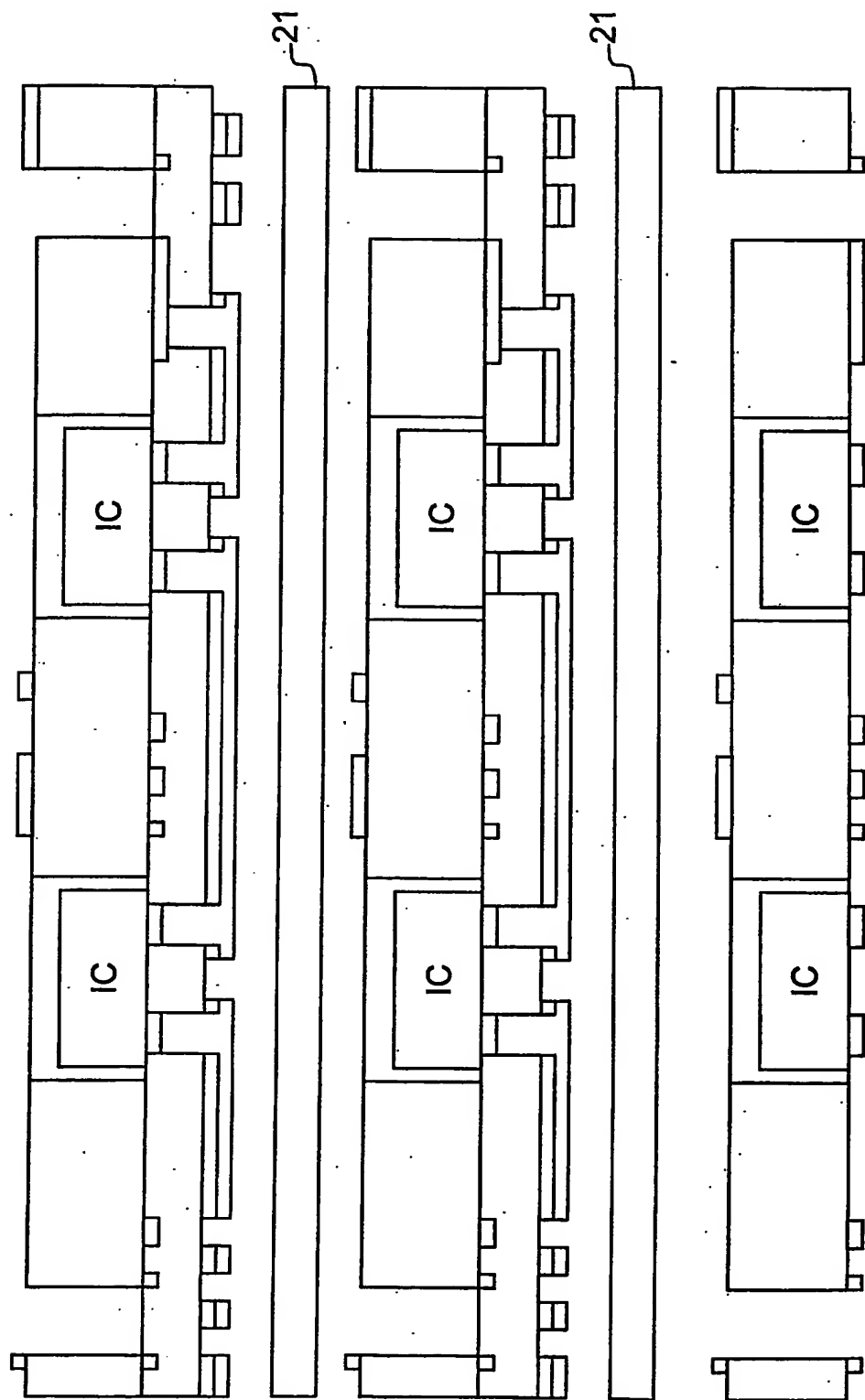


Fig. 2A

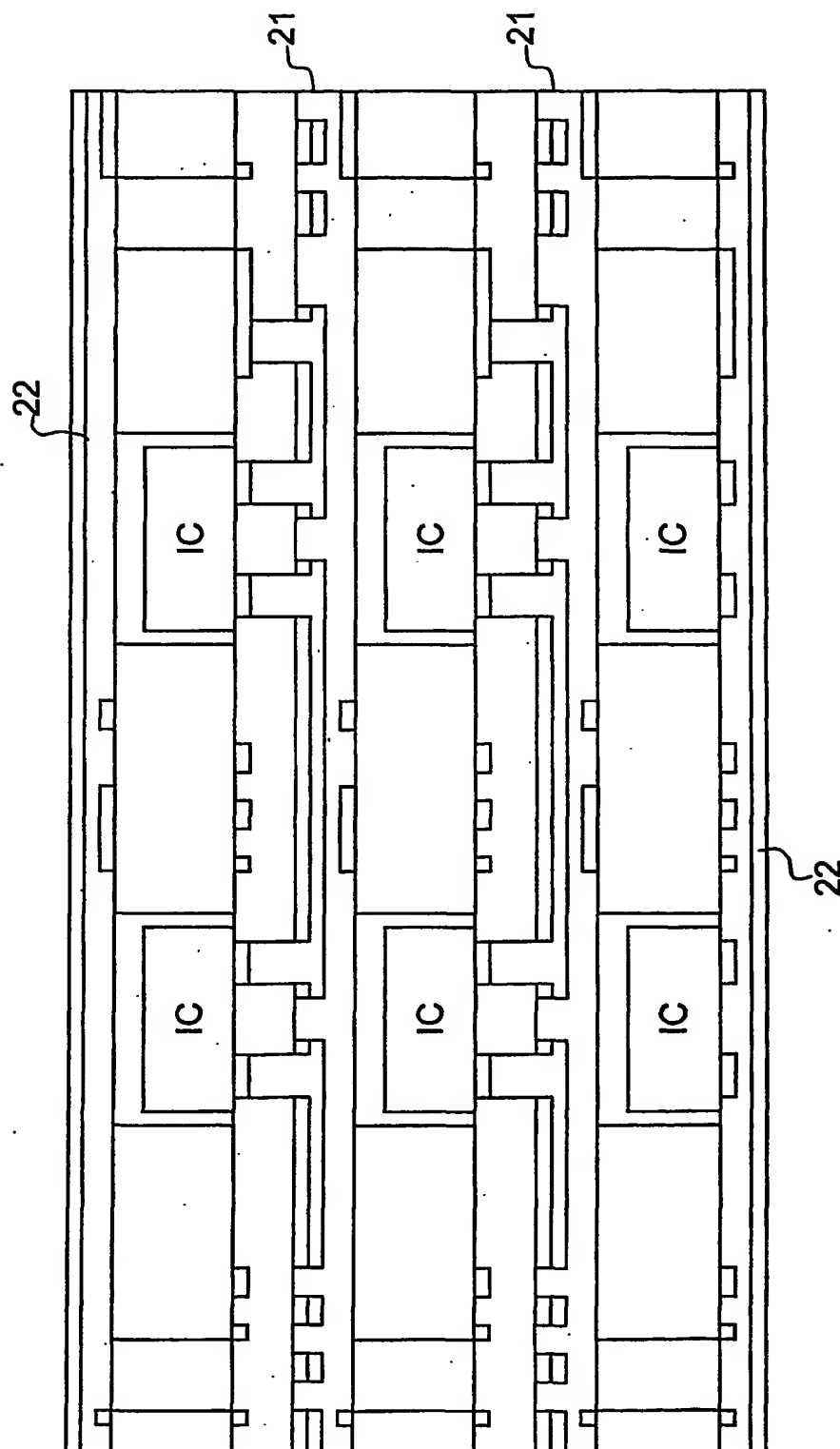


Fig. 2B

9/11

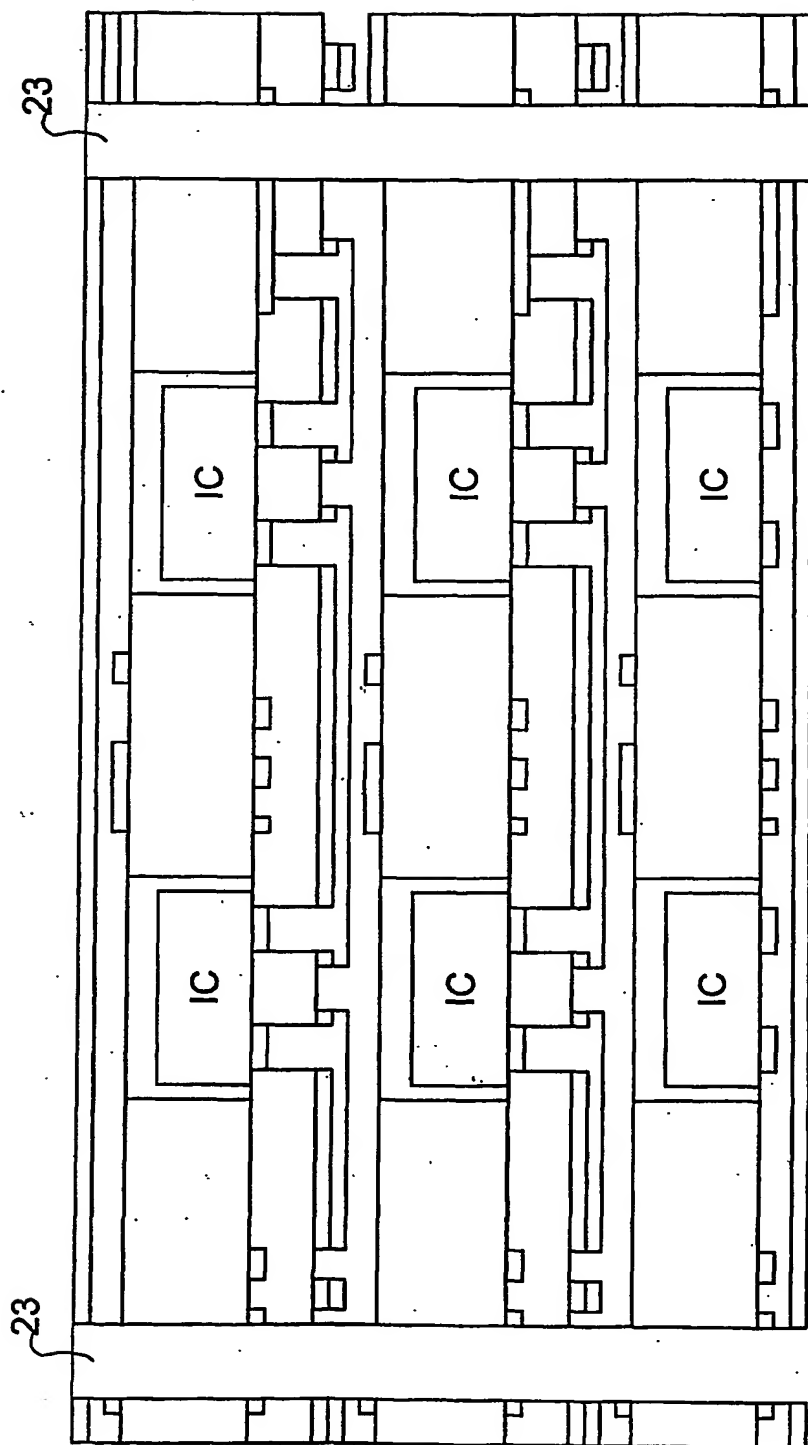


Fig. 2C

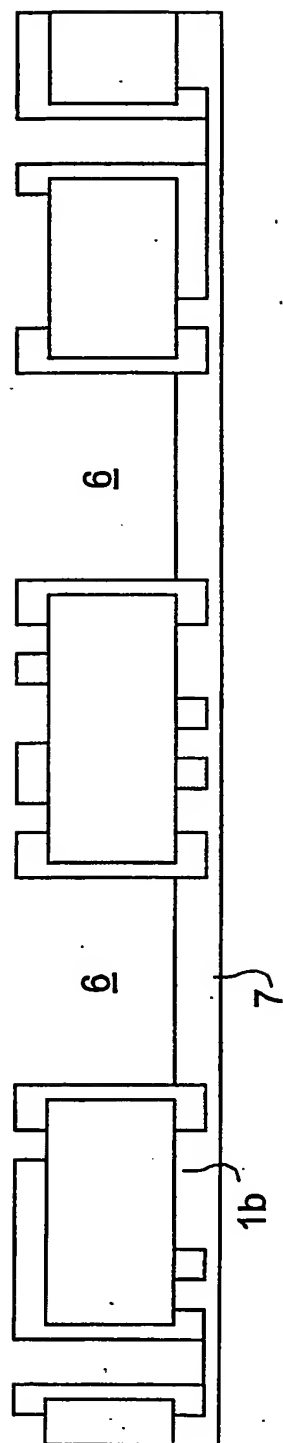


Fig. 3A

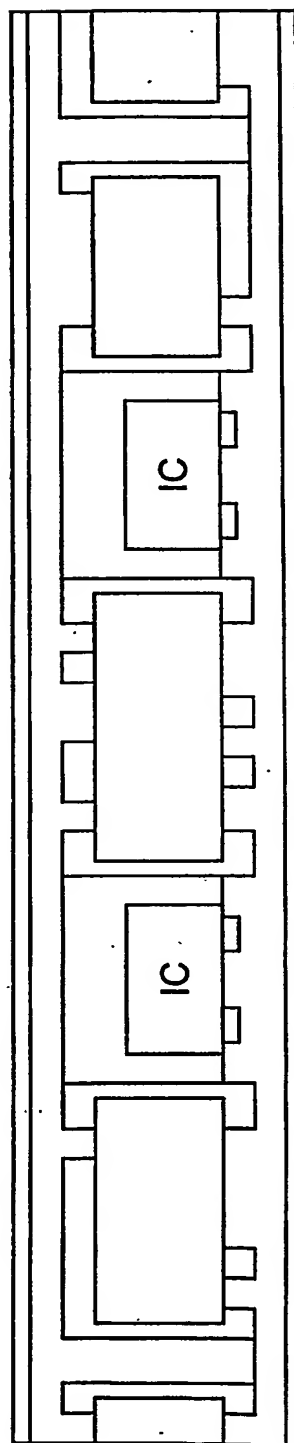


Fig. 3B

11/11

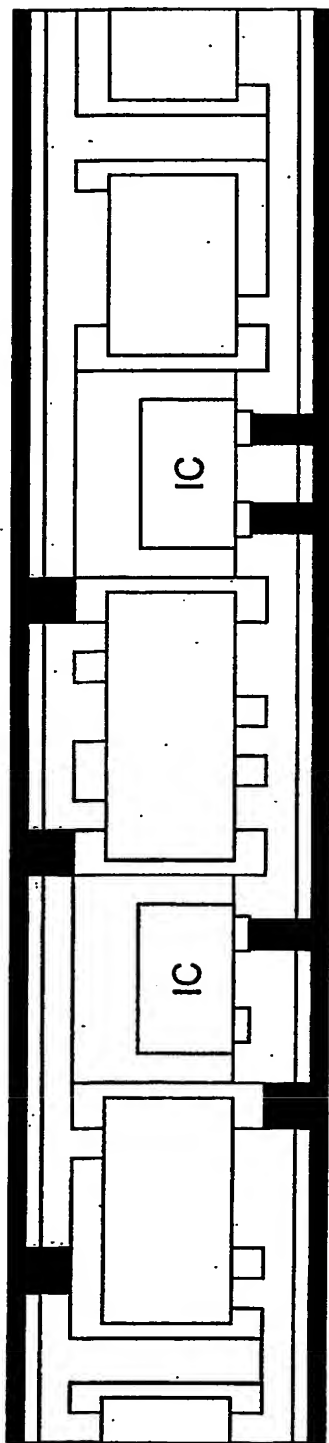


Fig. 3C

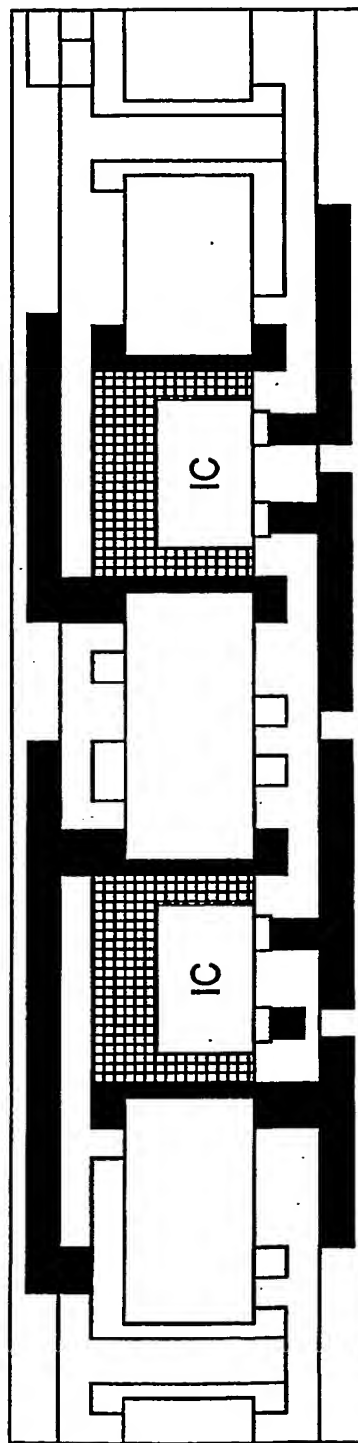


Fig. 3D

INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI 03/00064

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H05K 1/18, H05K 3/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI DATA, EPO-INTERNAL, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5306670 A (LARRY J. MOWATT ET AL), 26 April 1994 (26.04.94), column 6, line 65 - column 8, line 32, figures 1-6 --	1-22
X	US 3192307 A (M. LAZAR), 29 June 1965 (29.06.65), see whole document --	1-10,12-14, 21-22
A	--	11,15-20
A	WO 0021344 A1 (TELEFONAKTIEBOLAGET LM ERICSSON), 13 April 2000 (13.04.00), see whole document -- -----	6,7,8,9

☐ Further documents are listed in the continuation of Box C.
 ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

2 May 2003

Date of mailing of the international search report

08-05-2003

Name and mailing address of the ISA/

Swedish Patent Office

Box 5055, S-102 42 STOCKHOLM

Facsimile No. +46 8 666 02 86

Authorized officer

Kerstin Waczinska/MN

Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

Information on patent family members

29/03/03

International application No.

PCT/FI 03/00064

Patent document cited in search report				Publication date		Patent family member(s)		Publication date	
US	5306670	A	26/04/94	JP	6350020	A		22/12/94	
US	5432677	A		US	6400573	B		11/07/95	
US	3192307	A	29/06/65	CH	411070	A		15/04/66	
FR	1397874	A		NL	6406045	A		30/04/65	
WO	0021344	A1	13/04/00	AU	1303900	A		26/04/00	
EP	1123643	A		SE	513341	C		21/08/00	
SE	9803392	A						07/04/00	

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☒ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.